

AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

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DI cont.  
1. (Original) An integrated circuit comprising:  
a temperature sensor providing a temperature measurement of the integrated circuit;  
a programmable storage location storing a first temperature limit value, the  
programmable storage location accessible via an instruction executed by the  
integrated circuit; and  
compare logic coupled to the temperature sensor and the storage location to provide an  
indication of a comparison between the temperature measurement and the first  
temperature limit value.

2. (Original) The integrated circuit as recited in claim 1 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.

3. (Original) The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.

4. (Original) The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, in response to access to a control location in the integrated circuit.

5. (Original) The integrated circuit as recited in claim 2 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement falls below a programmable second temperature limit value or when a control location in the integrated circuit is accessed, according to a programmable mode of operation.

6. (Original) The integrated circuit as recited in claim 2 wherein the first temperature limit value is a panic value indicating a temperature limit for safe integrated circuit operation.

7. (Currently Amended) The integrated circuit as recited in claim 1 further comprising an addressable storage location coupled to the temperature sensor, the addressable storage location accessible by an instruction executed by the integrated circuit and supplying an indication of the temperature measurement on the integrated circuit.

D<sup>1</sup> 8. (Previously presented) The integrated circuit as recited in claim 2 further comprising: a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature measurement indicated by the temperature sensor is above a second temperature limit value.

9. (Original) The integrated circuit as recited in claim 8 further comprising: a second storage location supplying the second temperature limit value; and second compare logic coupled to the second storage location and coupled to receive the temperature measurement of the integrated circuit, and wherein the second compare logic generates a second indication of when the temperature measurement of the integrated circuit is above the second temperature limit value.

10. (Original) The integrated circuit as recited in claim 9 further comprising: a third storage location supplying a third temperature limit value; third compare logic coupled to the third storage location and coupled to receive the temperature measurement, and wherein the compare logic generates a third indication that the temperature measurement of the integrated circuit is below the third temperature limit value.

11. (Currently Amended) The integrated circuit as recited in claim [[1]] 10 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement indicated by the temperature sensor is below the third temperature limit value.

12. (Original) The integrated circuit as recited in claim 1 wherein the integrated circuit is a microprocessor.

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13. (Currently Amended) A method comprising:  
measuring a temperature of an integrated circuit with a temperature sensor, the  
temperature sensor being a circuit within the integrated circuit;  
comparing the measured temperature to a first limit value stored in the integrated circuit;  
and  
generating a signal on a first output terminal of the integrated circuit according to the  
comparison to control the temperature of the integrated circuit, wherein  
the signal is asserted when the measured temperature is greater than the first limit value,  
and wherein  
the signal on the first output terminal is deasserted ~~when~~ in response to either a control  
location on the integrated circuit is being accessed or ~~when~~ the measured  
temperature ~~goes~~ falling below a lower limit value, according to a programmable  
mode of operation.

14. Canceled.

15. (Previously presented) The method as recited in claim 13 wherein the asserted signal is used to inhibit a cooling device to control the temperature of the integrated circuit.

16. Canceled.

17. Canceled.

18. (Currently amended) The method as recited in claim ~~16~~ 13 wherein the signal is utilized to directly control a cooling device.

19. Canceled.

20. (Previously presented) A method comprising:

measuring a temperature of an integrated circuit with a temperature sensor, the  
 temperature sensor being a circuit within the integrated circuit;  
 comparing the measured temperature to a first limit value stored in the integrated circuit;  
 generating a signal on a first output terminal of the integrated circuit according to the  
 comparison to control the temperature of the integrated circuit; and  
 accessing a control location in the integrated circuit to cause the signal to be deasserted.

21. (Previously presented) The method as recited in claim 13 wherein the asserted signal causes assertion of an interrupt and wherein a sequence of instructions, responsive to the asserted interrupt, activates a cooling device.

22. (Original) The method as recited in claim 21 wherein an instruction sequence causes the signal to be deasserted.

23. (Previously presented) A method comprising:  
 measuring a temperature of an integrated circuit with a temperature sensor, the  
 temperature sensor being a circuit within the integrated circuit;  
 comparing the measured temperature to a first limit value stored in the integrated circuit;  
 and  
 generating a signal on a first output terminal of the integrated circuit according to the  
 comparison to control the temperature of the integrated circuit;  
 comparing the measured temperature to a second limit value stored in the integrated  
 circuit; and  
 asserting a second signal on a second output terminal of the integrated circuit when the  
 measured temperature is above the second limit value, thereby indicating that  
 temperature has exceeded a safe limit.

24. (Original) The method as recited in claim 23 wherein the second signal is deasserted by accessing a control location in the integrated circuit.

25. (Currently Amended) An apparatus comprising:  
 a processor including,

means for measuring a temperature of the processor and providing a measured temperature;

means for comparing the measured temperature to at least ~~two limit values~~ a first limit value and a second limit value; and

~~two output terminals on the processor coupled to supply an indication of results the comparison.~~

means for providing a control signal on a first output terminal of the processor according to the comparison of the measured temperature to the first limit value, the control signal to control the temperature of the integrated circuit; and

means for providing an indicator signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that the measured temperature has exceeded a safe limit.

26. (Original) The apparatus as recited in claim 25 wherein the apparatus is a computer system and further comprises at least one cooling device, which activates in response to an asserted signal on at least one of the two output terminals.

27. (Original) A microprocessor comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

at least a first and second temperature limit value stored in programmable storage

locations in the microprocessor, the storage locations being accessible via software executed by the microprocessor;

compare logic coupled to the temperature sensor and to the programmable storage

locations storing the first and second temperature limit values, to provide

respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values; and

first and second output terminals coupled to provide respectively, the first and second signals.

28. (Original) The microprocessor as recited in claim 27 wherein the microprocessor deasserts the first signal, which is supplied on the first output terminal of processor, when the temperature measurement falls below a programmable third temperature limit value, thereby providing a thermostat mode of operation for the first signal.

29. (Original) The integrated circuit as recited in claim 27 wherein the microprocessor includes a software accessible control register controlling operation of the compare logic and the first and second output terminals.

30. (New) An integrated circuit comprising:  
a temperature sensor to provide a measured temperature of the integrated circuit;  
a storage location to hold a first programmable value indicating a first temperature limit;  
and  
compare logic coupled to compare the measure temperature and the first temperature limit and to provide an indication of the comparison.

31. (New) The integrated circuit as recited in claim 30 further comprising a first output coupled to provide a first temperature control signal corresponding to the indication provided by the compare logic.

32. (New) The integrated circuit as recited in claim 31 wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to an indication that the measured temperature does not exceed the first temperature limit.

33. (New) The integrated circuit as recited in claim 31 further including a second storage location to hold a second programmable value indicating a second temperature limit, and wherein the compare logic is further to compare the measured temperature and the second temperature limit and to provide a second indication thereof.

34. (New) The integrated circuit as recited in claim 33 wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to the second indication that the measured temperature does not exceed the second temperature limit.

35. (New) The integrated circuit as recited in claim 33, further comprising a second output coupled to provide an indicator signal in response to the second indication provided by the compare logic, wherein the indicator signal indicates that the integrated circuit has exceeded the second temperature limit.

36. (New) The integrated circuit as recited in claim 31 further comprising a third storage location to hold a control value, and wherein a state of the first temperature control signal is controlled, at least in part by the control value.

37. (New) The integrated circuit as recited in claim 36, wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to the control value.

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